CMOS RESET IC

BD48XXG/FVE
BD49XXG/FVE

Rohm's BD48XXG/FVE and BD49XXG/FVE are series of high-accuracy, low-power VOLTAGE DETECTOR ICs with a CMOS process. For flexible choice according to the application, BD48XXG/FVE series with N channel open drain output and BD49XXG/FVE series with CMOS output are available in 38 voltage types from 2.3 V to 6.0 V in steps of 0.1 V in different packages, totaling 152 models.

●Applications

Every kind of appliances with microcontroller and logic circuit

●Features

1) Detection voltage: 0.1V step line-up 2.3~6.0V (Typ.)
2) High-accuracy detection voltage: ±1.5% Max.
3) Ultra low current consumption: 0.8μA typ. (Output is High.)
4) Nch open drain output (BD48XXG/FVE series),
   CMOS output (BD49XXG/FVE series)
5) Small package VSOF5(EMP5) : BD48XXFVE/BD49XXFVE
   SSOP5(SMP5C2) : BD48XXG/BD49XXG

●Selection guide

For BD4XXXX series, detection voltage, output circuit types (Refer to the block diagram at P3), and package (Refer to the dimension at P14) can be selected for your own application.
Part number of devices for each specification is shown below.

Part No. : B D 4 X X X X
① ② ③

Part No.	Specification	Contents
①	Output circuit types	8 : Open drain output 9 : CMOS output
②	Detection voltage	Ex. : Vs : described in each 0.1V step for 2.3V~6.0V range (29 means 2.9V)
③	Package	G : SSOP5 (SMP5C2) FVE : VSOF5 (EMP5)

●Line-up

Detection voltage Vs	Nch Open drain output (BD48XXG/FVE)	CMOS output (BD49XXG/FVE)	Detection voltage Vs (V) Ta=25˚C			Hysteresis voltage (V,Typ.)	Package
			Min.	Typ.	Max.		
6.0V	BD4860G/FVE	BD4960G/FVE	5.910	6.000	6.090	Vs X 0.05	SSOP5 (SMP5C2) / VSOF5 (EMP5)
5.9V	BD4859G/FVE	BD4959G/FVE	5.812	5.900	5.989		SSOP5 (SMP5C2) / VSOF5 (EMP5)
5.8V	BD4858G/FVE	BD4958G/FVE	5.713	5.800	5.887		SSOP5 (SMP5C2) / VSOF5 (EMP5)
5.7V	BD4857G/FVE	BD4957G/FVE	5.615	5.700	5.786		SSOP5 (SMP5C2) / VSOF5 (EMP5)
5.6V	BD4856G/FVE	BD4956G/FVE	5.516	5.600	5.684		SSOP5 (SMP5C2) / VSOF5 (EMP5)
5.5V	BD4855G/FVE	BD4955G/FVE	5.418	5.500	5.583		SSOP5 (SMP5C2) / VSOF5 (EMP5)
5.4V	BD4854G/FVE	BD4954G/FVE	5.319	5.400	5.481		SSOP5 (SMP5C2) / VSOF5 (EMP5)
5.3V	BD4853G/FVE	BD4953G/FVE	5.221	5.300	5.380		SSOP5 (SMP5C2) / VSOF5 (EMP5)
5.2V	BD4852G/FVE	BD4952G/FVE	5.122	5.200	5.278		SSOP5 (SMP5C2) / VSOF5 (EMP5)
5.1V	BD4851G/FVE	BD4951G/FVE	5.024	5.100	5.177		SSOP5 (SMP5C2) / VSOF5 (EMP5)
5.0V	BD4850G/FVE	BD4950G/FVE	4.925	5.000	5.075		SSOP5 (SMP5C2) / VSOF5 (EMP5)
4.9V	BD4849G/FVE	BD4949G/FVE	4.827	4.900	4.974		SSOP5 (SMP5C2) / VSOF5 (EMP5)
4.8V	BD4848G/FVE	BD4948G/FVE	4.728	4.800	4.872		SSOP5 (SMP5C2) / VSOF5 (EMP5)
4.7V	BD4847G/FVE	BD4947G/FVE	4.630	4.700	4.771		SSOP5 (SMP5C2) / VSOF5 (EMP5)
4.6V	BD4846G/FVE	BD4946G/FVE	4.531	4.600	4.669		SSOP5 (SMP5C2) / VSOF5 (EMP5)
4.5V	BD4845G/FVE	BD4945G/FVE	4.433	4.500	4.568		SSOP5 (SMP5C2) / VSOF5 (EMP5)
4.4V	BD4844G/FVE	BD4944G/FVE	4.334	4.400	4.466		SSOP5 (SMP5C2) / VSOF5 (EMP5)
4.3V	BD4843G/FVE	BD4943G/FVE	4.236	4.300	4.365		SSOP5 (SMP5C2) / VSOF5 (EMP5)
4.2V	BD4842G/FVE	BD4942G/FVE	4.137	4.200	4.263		SSOP5 (SMP5C2) / VSOF5 (EMP5)
4.1V	BD4841G/FVE	BD4941G/FVE	4.039	4.100	4.162		SSOP5 (SMP5C2) / VSOF5 (EMP5)
4.0V	BD4840G/FVE	BD4940G/FVE	3.940	4.000	4.060		SSOP5 (SMP5C2) / VSOF5 (EMP5)
3.9V	BD4839G/FVE	BD4939G/FVE	3.842	3.900	3.959		SSOP5 (SMP5C2) / VSOF5 (EMP5)
3.8V	BD4838G/FVE	BD4938G/FVE	3.743	3.800	3.857		SSOP5 (SMP5C2) / VSOF5 (EMP5)
3.7V	BD4837G/FVE	BD4937G/FVE	3.645	3.700	3.756		SSOP5 (SMP5C2) / VSOF5 (EMP5)
3.6V	BD4836G/FVE	BD4936G/FVE	3.546	3.600	3.654		SSOP5 (SMP5C2) / VSOF5 (EMP5)
3.5V	BD4835G/FVE	BD4935G/FVE	3.448	3.500	3.553		SSOP5 (SMP5C2) / VSOF5 (EMP5)
3.4V	BD4834G/FVE	BD4934G/FVE	3.349	3.400	3.451		SSOP5 (SMP5C2) / VSOF5 (EMP5)
3.3V	BD4833G/FVE	BD4933G/FVE	3.251	3.300	3.350		SSOP5 (SMP5C2) / VSOF5 (EMP5)
3.2V	BD4832G/FVE	BD4932G/FVE	3.152	3.200	3.248		SSOP5 (SMP5C2) / VSOF5 (EMP5)
3.1V	BD4831G/FVE	BD4931G/FVE	3.054	3.100	3.147		SSOP5 (SMP5C2) / VSOF5 (EMP5)
3.0V	BD4830G/FVE	BD4930G/FVE	2.955	3.000	3.045		SSOP5 (SMP5C2) / VSOF5 (EMP5)
2.9V	BD4829G/FVE	BD4929G/FVE	2.857	2.900	2.944		SSOP5 (SMP5C2) / VSOF5 (EMP5)
2.8V	BD4828G/FVE	BD4928G/FVE	2.758	2.800	2.842		SSOP5 (SMP5C2) / VSOF5 (EMP5)
2.7V	BD4827G/FVE	BD4927G/FVE	2.660	2.700	2.741		SSOP5 (SMP5C2) / VSOF5 (EMP5)
2.6V	BD4826G/FVE	BD4926G/FVE	2.561	2.600	2.639		SSOP5 (SMP5C2) / VSOF5 (EMP5)
2.5V	BD4825G/FVE	BD4925G/FVE	2.463	2.500	2.538		SSOP5 (SMP5C2) / VSOF5 (EMP5)
2.4V	BD4824G/FVE	BD4924G/FVE	2.364	2.400	2.436		SSOP5 (SMP5C2) / VSOF5 (EMP5)
2.3V	BD4823G/FVE	BD4923G/FVE	2.266	2.300	2.335		SSOP5 (SMP5C2) / VSOF5 (EMP5)

●Pin layout

Pin layout of VSOF5(EMP5) and SSOP5(SMP5C2) is different as shown below. (Fig.1, Fig.2)
When used as replacement, please consider the difference. (The detail of packages is shown at P14.)

BD48XXFVE/BD49XXFVE

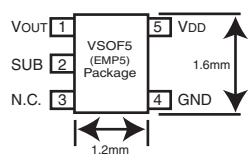


Fig.1

BD48XXG/BD49XXG

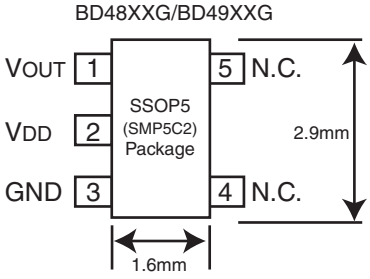


Fig.2

(Note) Connect SUB pin with GND pin.

● Block diagram

Two output types can be used. One is BD48XXG/FVE (Fig.3) of open drain output type, and the other is BD49XXG/FVE (Fig.4) of CMOS output type.

BD48XXG/FVE : Open drain output

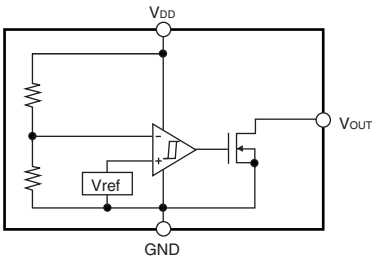


Fig.3

BD49XXG/FVE : CMOS output

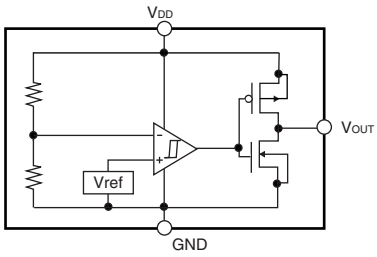


Fig.4

● Absolute maximum rating (Ta=25˚C)

To prevent the functional deterioration or thermal damage of semiconductor devices and ensure their service life and reliability, they must be designed and reviewed in such a way that the absolute maximum rating can not be exceeded in any cases or even at any moment.

Parameter		Symbol	Limits	Unit
Power supply voltage		VDD – GND	– 0.3 ~ + 10	V
Output voltage	Nch Open drain output	VOUT	GND – 0.3 ~ + 10	V
	CMOS output		GND – 0.3 ~ VDD + 0.3	
Power dissipation	SSOP5 (SMP5C2) *1 *3	Pd	150	mW
Power dissipation	VSOF5 (EMP5) *2 *3	Pd	100	mW
Operating temperature		Topr	– 40 ~ + 85	˚C
Storage temperature		Tstg	– 55 ~ + 125	˚C

*1 Derating : 1.5mW/˚C for operation above Ta=25˚C
*2 Derating : 1.0mW/˚C for operation above Ta=25˚C
*3 When only IC is used.

• Power supply voltage

This voltage is the applied voltage between VDD and GND. The applied voltage should not exceed the indicated value.

• Output voltage

VOUT pin voltage should not exceed the indicated value. For Nch open drain output type, VDD applied voltage and VOUT pin H output voltage can be used independently. Both of them should not exceed the each indicated value.

• Operating temperature range

The circuit function is guaranteed within the temperature range. However, the operating characteristics are different from that of Ta=25˚C. If they are any questions about the extent of guarantee of circuit functions in this operating temperature range, please ask for more technical information.

• Storage temperature range

This IC can be stored up to this temperature range without deterioration of characteristics. However, an abrupt thermal shock of extreme temperature fluctuations may cause the deterioration of characteristics.

● Power dissipation

Power consumption of the IC

Circuit current at ON/OFF is very small. Power consumption in output depends on each load connected with VOUT pin. Please note that total power consumption must be within a power dissipation range in the secure area of the entire operating temperature. Power dissipation of these packages; SSOP5 (SMP5C2) package (BD48XXG/BD49XXG) Fig.5, and VSOF5 (EMP5) package (BD48XXFVE/BD49XXFVE) Fig.6 is shown below.

SSOP5 (SMP5C2) package

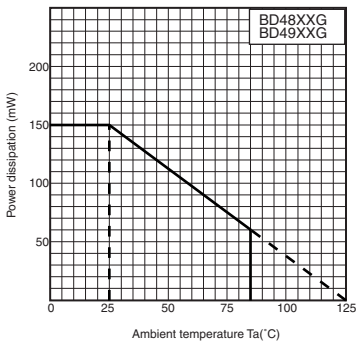


Fig.5 Thermal derating curve

EMP5 (VSOF5) package

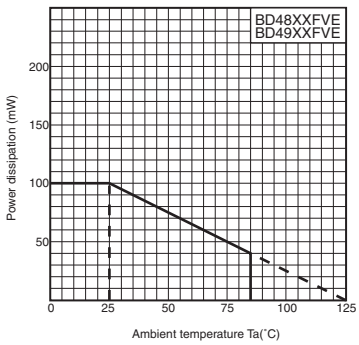


Fig.6 Thermal derating curve

When it is used in the ambient temperature of (Ta)=25˚C and more, make reference to each thermal derating characteristics of used package. Both Fig.5 and Fig.6 show these characteristic when only IC is used.

● Electrical characteristics (Unless otherwise noted; Ta=-25˚C ~ 85˚C)

Parameter	Symbol	Min.	Tap.	Max.	Unit	Conditions		Reference
Detection voltage temperature coefficient	Vs/ΔT	—	±100	±360	ppm/˚C			Fig.33
Hysteresis voltage	ΔVs	Vs x 0.03	Vs x 0.05	Vs x 0.08	V	RL=470kΩ, VDD=L→H→L		Fig.31
"H" transfer delay time	TPLH	—	—	100	μs	CL=100pF, RL=100kΩ *2 VOUT=GND→ 50% *1		Fig.12,13 15,17
Circuit current when ON	ICC1	—	0.51	1.53	μA	VDD=Vs–0.2V *1	Vs=2.3~3.1V	Fig.28
		—	0.56	1.68			Vs=3.2~4.2V	
		—	0.60	1.80			Vs=4.3~5.2V	
		—	0.66	1.98			Vs=5.3~6.0V	
Circuit current when OFF	ICC2	—	0.75	2.25	μA	VDD=Vs+2V *1	Vs=2.3~3.1V	
		—	0.80	2.40			Vs=3.2~4.2V	
		—	0.85	2.55			Vs=4.3~5.2V	
		—	0.90	2.70			Vs=5.3~6.0V	
Min. operating voltage	VOPL	0.95	—	—	V	RL=470kΩ, VOL≧0.4V *1		Fig.31
"L" output current	IOL	0.4	1	—	mA	VDS=0.5V, VDD=1.2V		Fig.29
		2.0	4	—		VDS=0.5V, VDD=2.4V (Vs≧2.7V)		
"H" output current	IOH	0.7	1.4	—	mA	VDS=0.5V, VDD=4.8V	Vs=2.3~4.2V	Fig.30
		0.9	1.8	—		VDS=0.5V, VDD=6.0V	Vs=4.3~5.2V	
		1.1	2.2	—		VDS=0.5V, VDD=8.0V	Vs=5.3~6.0V	
Output leak current	Ileak	—	—	0.1	μA	VDD=VDS=10V *1		Fig.32

*1 Operation is guaranteed forTa=25˚C.
*2 TPLH : VDD=(Vs typ.–0.5V)→ (Vs typ.+0.5V).
Note) RL is not necessary for CMOS output type.
Note) Minimum operating voltage
VOUT output becomes inconsistent if the VDD is equal to or lower than the operating limit voltage. It goes open, H, or L.
Note) Hysteresis voltage=(Reset release voltage)-(Reset detection voltage) [V]

● Term explanation

- Detection voltage (Vs) : VDD voltage when the output (Vout) goes from "H" to "L".
- Release voltage (Vs+ΔVs) : VDD voltage when output (Vout) goes from "L" to "H".
- Hysteresis voltage : The difference between detection voltage and release voltage. Malfunction due to noise in VDD (within hysteresis voltage) could be avoided by hysteresis voltage.

● Operating explanation

Ex.) For both open drain type (Fig.7) and CMOS output type (Fig.8), detection voltage and release voltage are threshold voltage. When voltage applied to VDD pin reaches each threshold voltage, VOUT pin voltage goes "H" →"L" or "L" →"H". BD48XXG/FVE series are open drain types and pull-up resistor must be connected to VDD, or other power supply. (In this case, output (VOUT) H voltage is VDD, or other power supply voltage.)

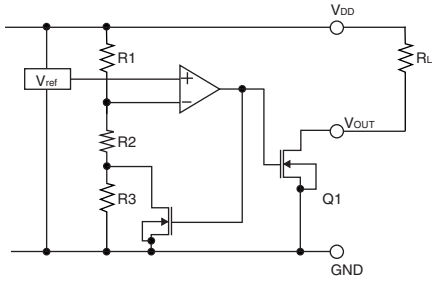


Fig.7 (BD48XX type Internal block diagram)

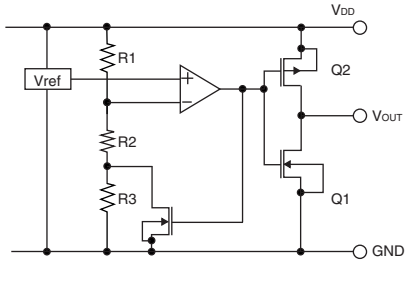


Fig.8 (BD49XX Internal block diagram)

• SWEEP DOWN for VDD

When VDD is equal to or more than the release voltage (Vs+ΔVs), output VOUT is in "H" mode. (Nch output transistor Q1 is OFF, Pch output transistor Q2 is ON.) When VDD is gradually decreased, output (VOUT) turns "L" in the detection voltage (Vs). (Nch output transistor Q1 is ON, Pch output transistor Q2 is OFF.)

• SWEEP UP for VDD

When VDD is equal to or lower than the detection voltage (Vs+ΔVs), output VOUT is in "L" mode. (Nch output transistor Q1 is ON, Pch output transistor Q2 is OFF.) When VDD is gradually increased, output (VOUT) turns "H" in the release voltage (Vs). (Nch output transistor Q1 is OFF, Pch output transistor Q2 is ON.)

• Some hysteresis is given such a way that the release voltage is the detection voltage X (1.05 Typ.).

• The output becomes inconsistent if the VDD is equal to or lower than the operating limit voltage.

● Timing waveform

Ex.) The relation between input voltage VDD and output voltage VOUT when VDD is increased and decreased is shown below. (Circuit is shown above. Fig7, 8)

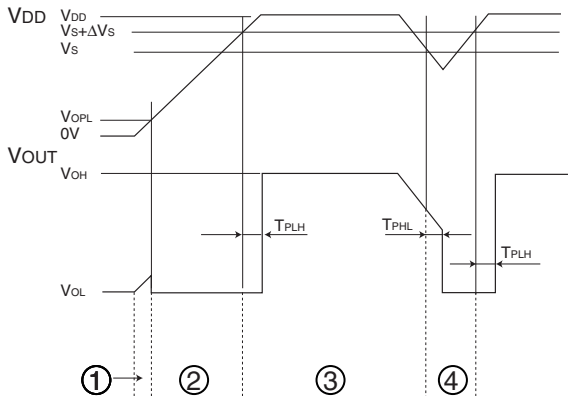


Fig.9

① If the VDD is equal to or lower than the operating limit voltage (VOPL) at power-up, the output is inconsistent.
② When the VDD is equal to or lower than the reset release voltage (Vs+ΔVs), VOUT=L.
③ When VDD exceeds the Reset Release Voltage, VOUT turns H with a delay of TPLH. See Fig. 15 and 17 for the reference waveform.
④ If the VDD goes below the detection (Vs) at power-down or instantaneous power failure, VOUT turns L with a delay of TPHL.

See Fig.16 and 18 for the reference waveform.
The potential difference between the detection voltage and the release voltage is called hysteresis (ΔVs).
The products are designed so as to prevent power supply fluctuation within this hysteresis from causing fluctuation in output in order to avoid malfunction due to noise.

● Application circuit

1)Application circuit as ordinal supply detection reset is shown below.

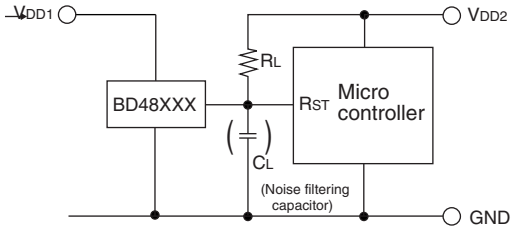


Fig.10 Open collector output type

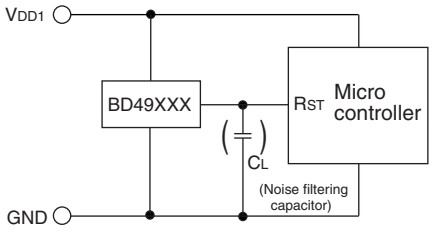


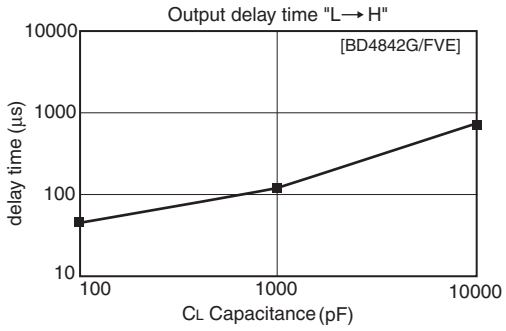
Fig.11 CMOS output type

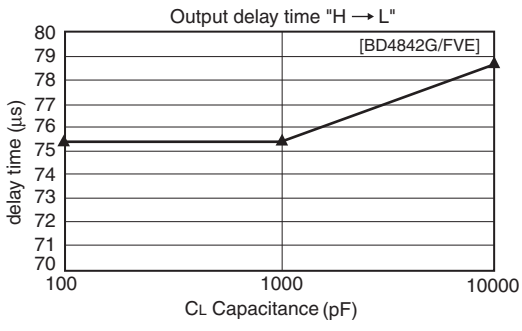
Output type of BD48XXG/FVE series (Open drain type) and BD49XXG/FVE series (CMOS type) is different. An example of usage is shown below.

- When the power supply of microcontroller (V_{DD2}) and power supply for the reset detection (V_{DD1}) is different. Provide R_L for the output of a product with open drain output (BD48XXG/FVE series) on the V_{DD2} side, as shown in Fig.10.

- When the power supply of microcontroller and that of reset is same (V_{DD1}). A product with CMOS output (BD49XXG/FVE series) can be used as shown in Fig.11. Or if R_L is provided with open drain output (BD48XXG/FVE series) on the V_{DD1} side, it can be used.

When the capacitor C_L for noise filtering and for delay time setting is connected to V_{OUT} pin (reset signal input pin of microcontroller), make a setting in consideration of the wave rounding of the rise and fall of V_{OUT}. (See the delay shown in Fig.14 as the reference.)





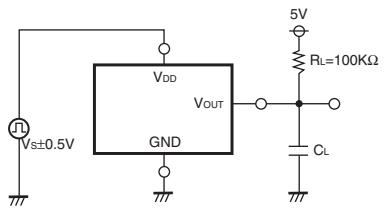


Fig.12

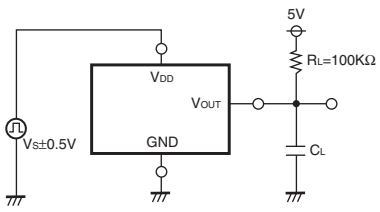


Fig.13

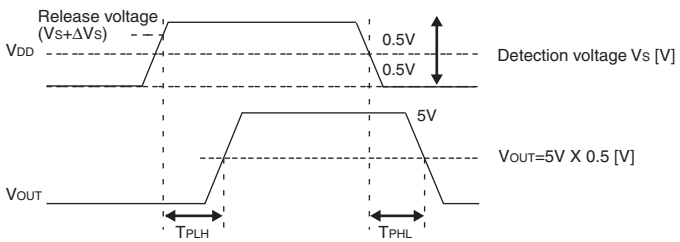


Fig.14 Delay time I/O condition

• Test data

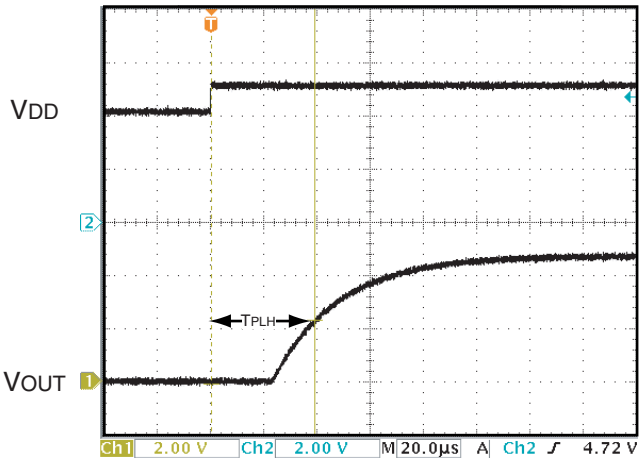


Fig.15
BD4845G TPLH output waveform

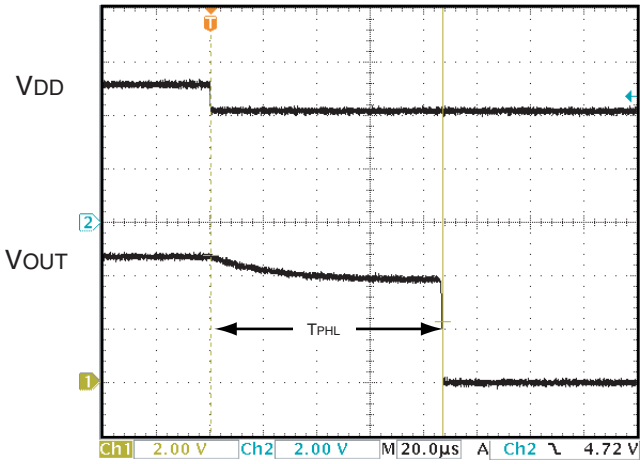


Fig.16
BD4845G TPHL output waveform

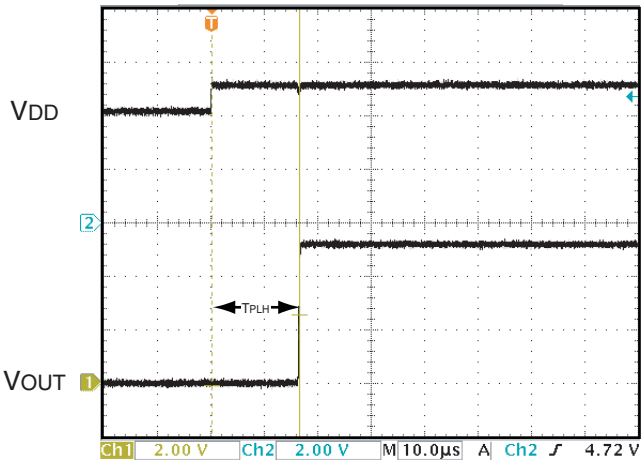


Fig.17
BD4945G TPLH output waveform

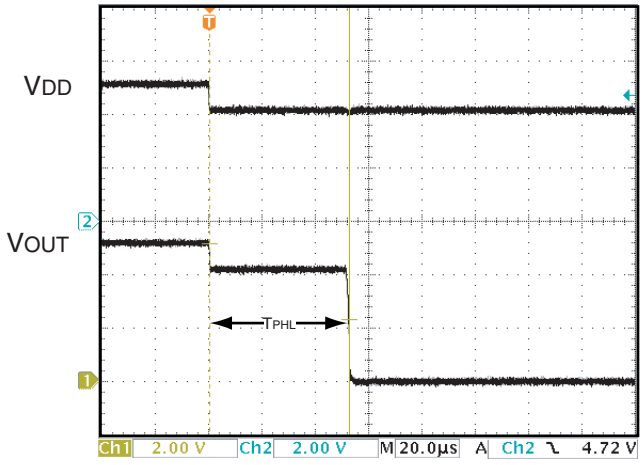
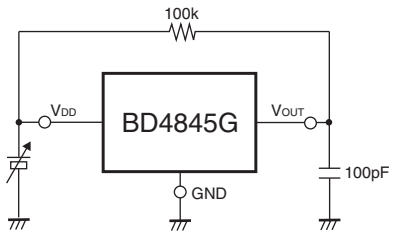
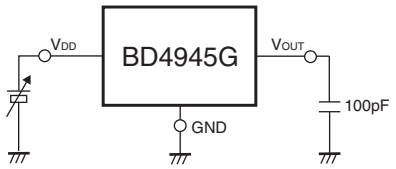


Fig.18
BD4945G TPHL output waveform

Reference data : BD4845G test data
RL=100kΩ
CL=100pF



Reference data : BD4945G test data
CL=100pF



2)Application circuit when microcontroller is reset with OR connection of the two types of the detection voltage is shown below.

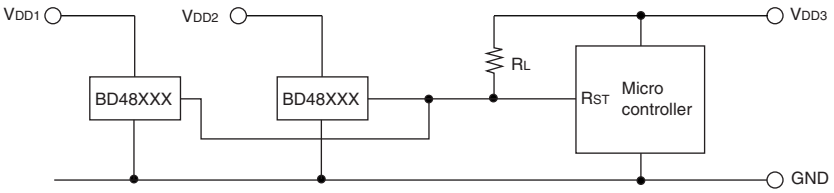


Fig.19

When there is more than one system power supply and it is necessary to individually monitor the power supply (V_{DD1}, V_{DD2}) to reset the microcontroller, open drain output type BD48XXG/FVE series can be connected to form an OR circuit as shown in Fig.19 for pulling up to an arbitrary voltage (V_{DD3}) to adjust the H voltage of the output to the microcontroller power supply (V_{DD3}).

3)Application circuit when it is used as Power-on reset is shown below.
(However, it can be used for only BD48XXG/FVE series.)

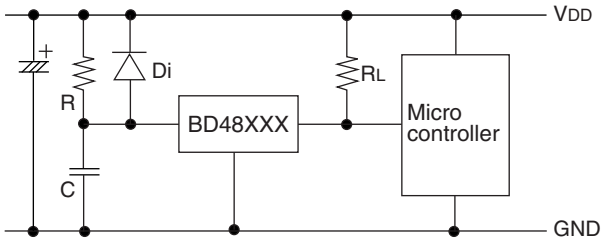


Fig.20

If the power supply voltage is lower than the guaranteed range, power-on reset of the microcontroller is necessary to prevent program runaways and unwanted memory register updates. A power-on reset circuit used with BD48XXG/FVE series (Nch open drain) is shown in Fig.20. C and R conneceted to V_{DD} pin of RESET IC make the wave rounding of the V_{DD} pin and generate input signal with time constant. When the input power supply is fallen, the electric charge of the capacitor is discharged through Di connected between V_{DD} pin and V_{DD}. The value of the resister R should be enough to prevent malfunction caused by circuit current through BD48XXG/FVE series. Set in such a way that the following expression stands:

Hysteresis > R X { (Circuit current at ON) - (Circuit current at OFF) }

Do not use BD49XXG/FVE series (CMOS output) for the power-on reset because malfunction may occur. (Oscillation at output etc.) The feed through current (CMOS output) at detection may cause malfunction mentioned above. (Feed through current is the current flowed from V_{DD} into GND instantly when output goes "H" ↔ "L".)

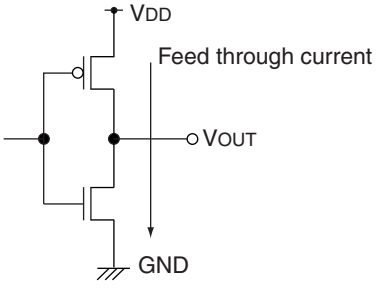


Fig.21
CMOS output circuit

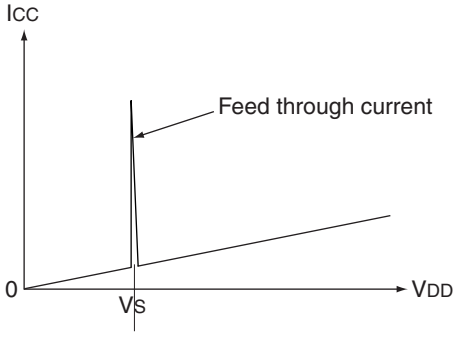


Fig.22
Current consumption Vs. power supply voltage

● Establishment of RESET transfer delay time

Delay time at the rise and fall of V_{DD} can be established by R_L, C_L connected to V_{OUT} pin.

• Delay time at the rise of V_{DD} T_{PLH} : Time until when V_{OUT} is 1/2 of V_{DD} after the rise of V_{DD}, and beyond the release voltage (Vs+ΔVs).(See P7). It is the total time established by IC internal transfer delay time T_D and external R_L, and C_L.

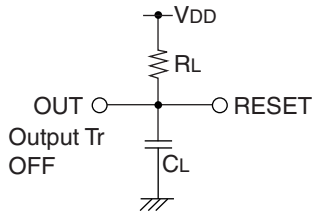


Fig.23

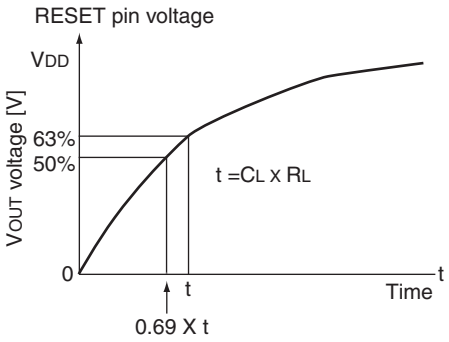


Fig.24 RESET pin voltage

If the threshold voltage of the RESET terminals is 1/2 of V_{CC}, delay time T_{PLH} at the rise of V_{DD} is shown in the expression below.

$T_{PLH}=0.69 \times C_L \times R_L+T_D$

T_D=Internal circuit delay of BD48XX : About 35μs (typ.) V_{DD}=(Vs–0.5V) → (Vs+0.5V)

C_L : Capacity of external capacitor beween V_{OUT} pin and GND

R_L : External resistance between V_{OUT} pin and power supply

• Delay time at the fall of V_{DD} T_{PHL} : Time until when V_{OUT} is 1/2 of V_{DD} after across the detection voltage (Vs).(See P7). It is the total time established by IC internal transfer delay time T_D and external R_L, and C_L.

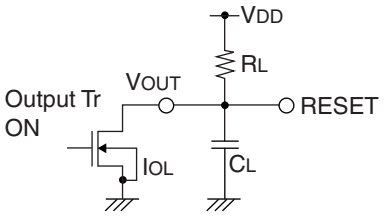


Fig.25

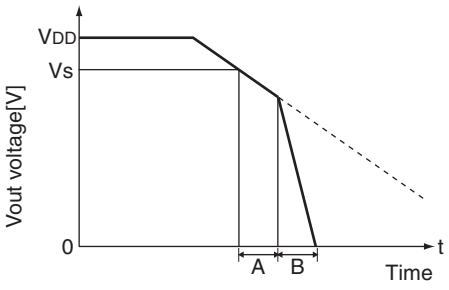


Fig.26 RESET pin voltage

$T_{PHL}=A+B$

A = About 70μs(Typ.) : Internal IC transfer delay time of BD4842

$B = \frac{CL \times Vs}{IOL}$: Delay time by external C_L, R_L

C_L : Capacity of external capacitor beween VOUT pin and GND

Vs : Detection voltage

I_{OL} : "L" output current of BD48XX

(Make sure to test in actual because it depends on detection voltage.
Reference:V_S=2.4V, V_{DD}=About 8mA at A:typ.)

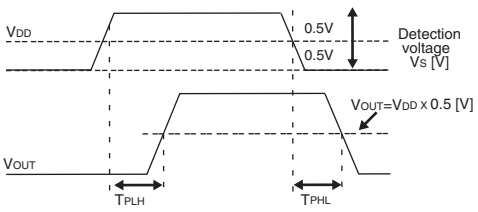


Fig.27 Delay time I/O condition

● Characteristic data (Reference data)

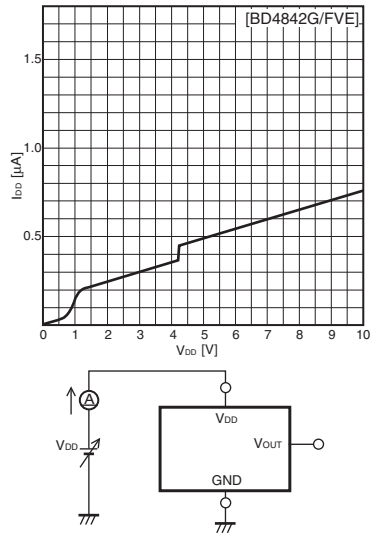


Fig.28
Circuit current

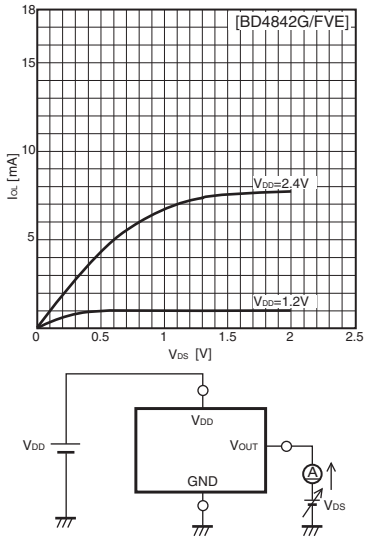


Fig.29
"L" output current

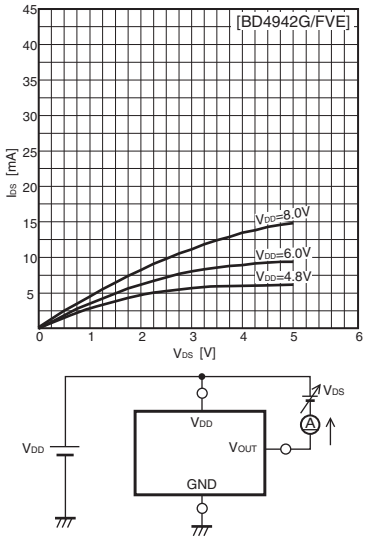


Fig.30
"H" output current

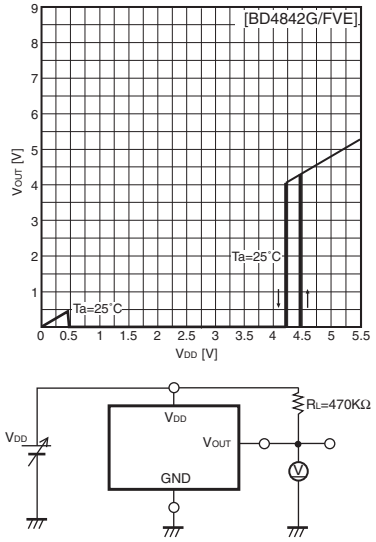


Fig.31
I/O characteristic

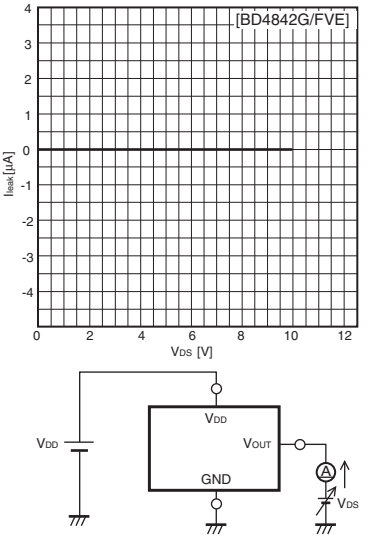


Fig.32
Output leak current

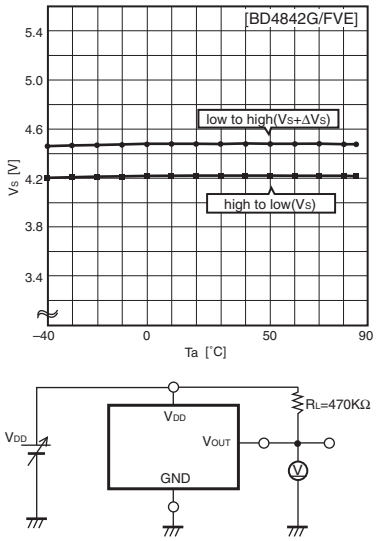


Fig.33
Detection voltage (Vs)
Release voltage (Vs+ΔVs)

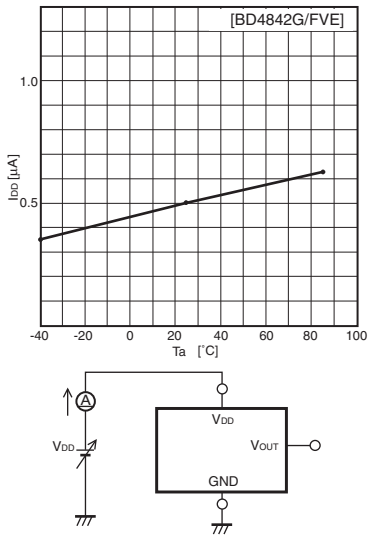


Fig.34
Circuit current on ON (Vs-0.2V)

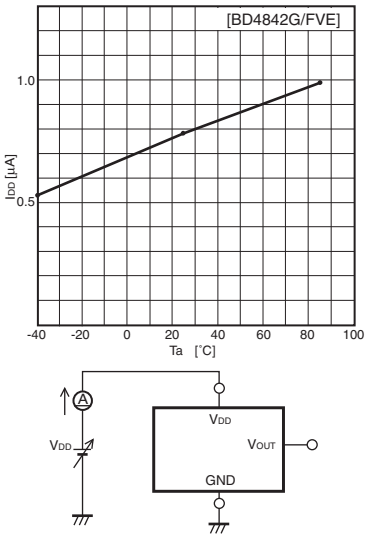


Fig.35
Circuit current on OFF (Vs+0.2V)

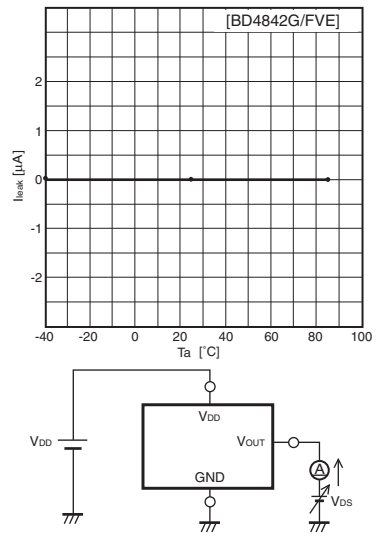


Fig.36
Output leak current

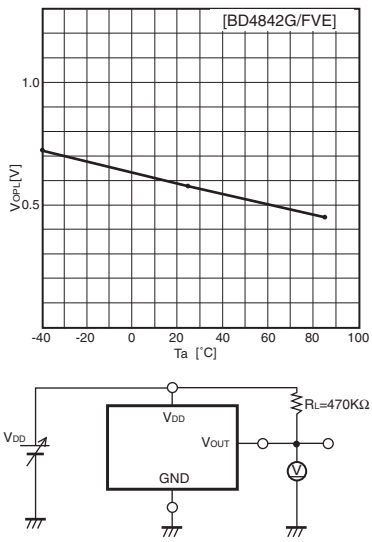


Fig.37
Operating limit voltage

● Taping specification

1)Dimension of tape

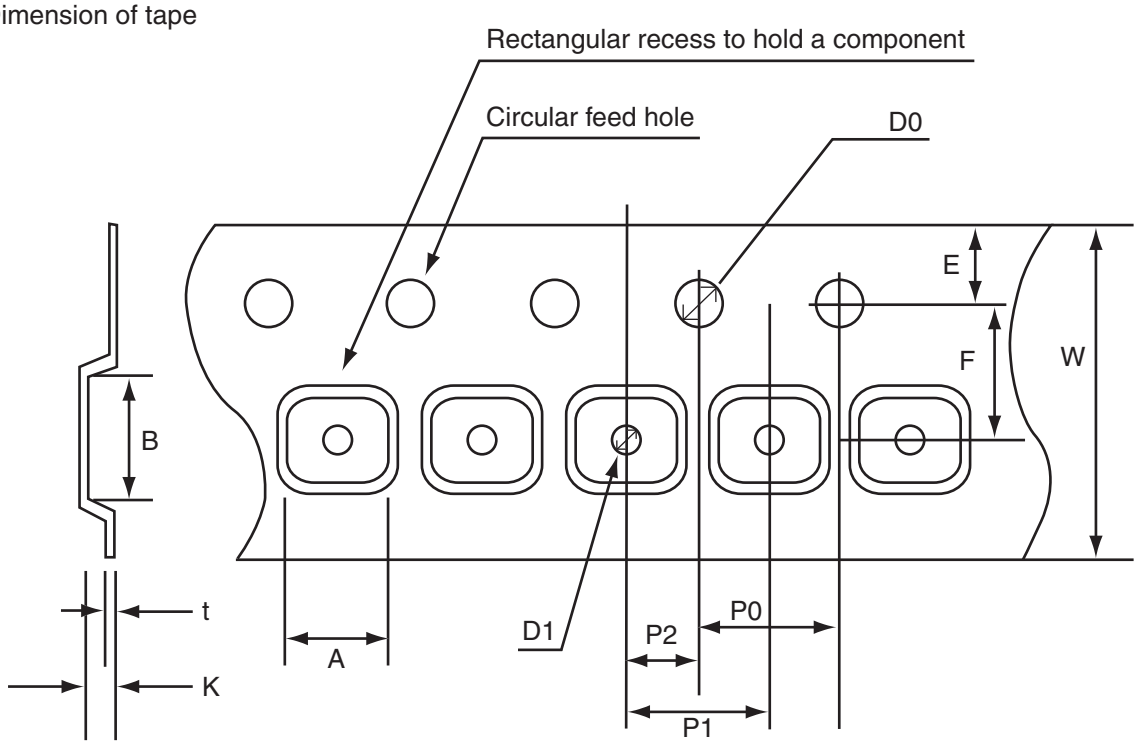


Fig.38

Package SSOP5 (SMP5C2)

(mm)

Symbol	A	B	D0	D1	E	F	P0	P1
Dimension	3.2±0.1	3.1±0.1	$1.5^{+0.1}_{-0}$	1.1±0.1	1.75±0.1	3.5±0.05	4.0±0.1	4.0±0.1

Symbol	P2	t	K	W
Dimension	2.0±0.05	0.3±0.05	1.3±0.1	8.0±0.2

Package VSOF5 (EMP5)

(mm)

Symbol	A	B	D0	D1	E	F	P0	P1
Dimension	1.83±0.1	1.83±0.1	$1.5^{+0.1}_{-0}$	0.5±0.1	1.75±0.1	3.5±0.05	4.0±0.1	4.0±0.1

Symbol	P2	t	K	W
Dimension	2.0±0.05	0.25±0.05	0.75±0.1	8.0±0.2

2)Dimension of reel

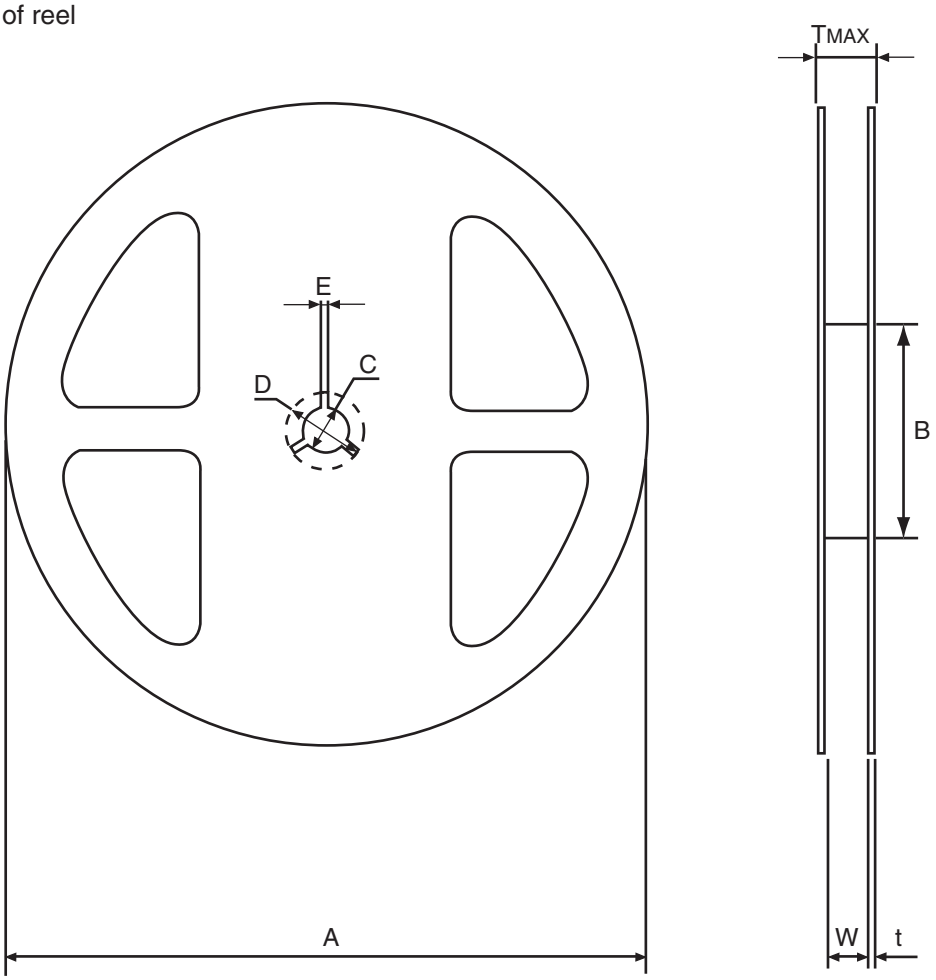


Fig.39

(mm)

Symbol	A	B	C	D	E	W	t	TMax.
Dimension	180 Max.	60±2.0	13.0±0.5	20.2 Min.	1.5 Min.	9.0±0.3	Label side(1.0) Back side(1.2)	17.4

3)Standard packaged quantity and IC direction

The standard packaged quantity is 3,000 pcs/reel. Orders should be in multiples of the standard packaged quantity. The ICs are TR oriented (as shown below).

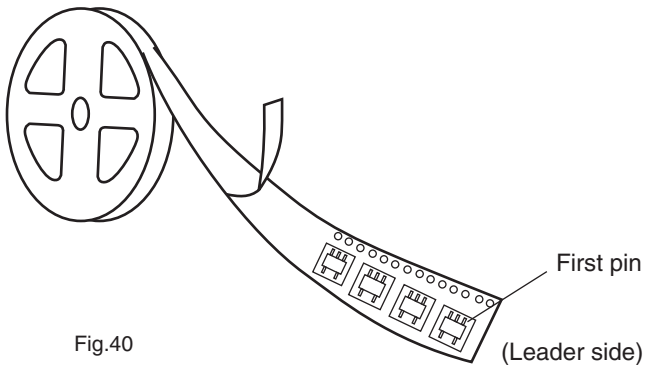
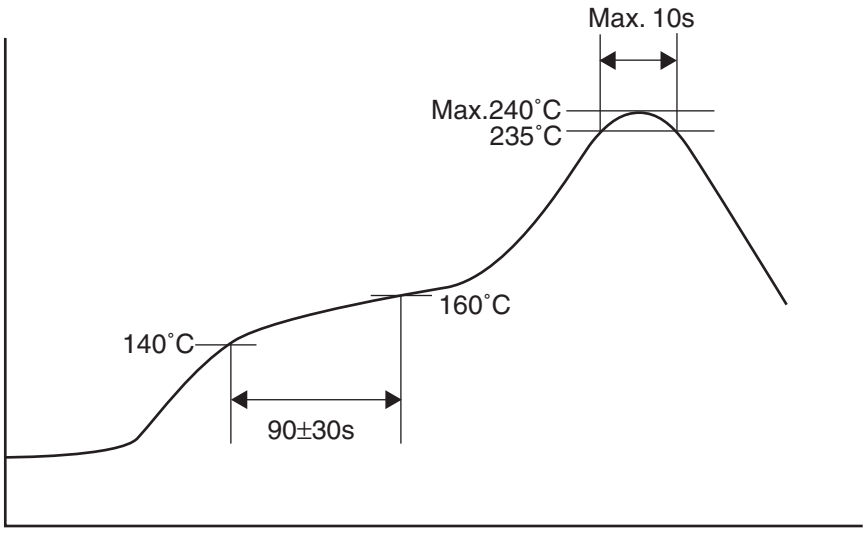


Fig.40

●Recommended mounting conditions

- SSOP5 (SMP5C2) allows either reflow or flow soldering mounting.
- VSOF5 (EMP5) allows reflow mounting.
  The mounting conditions are shown below.

1)Reflow



Up to two reflows are allowed.

Fig.41

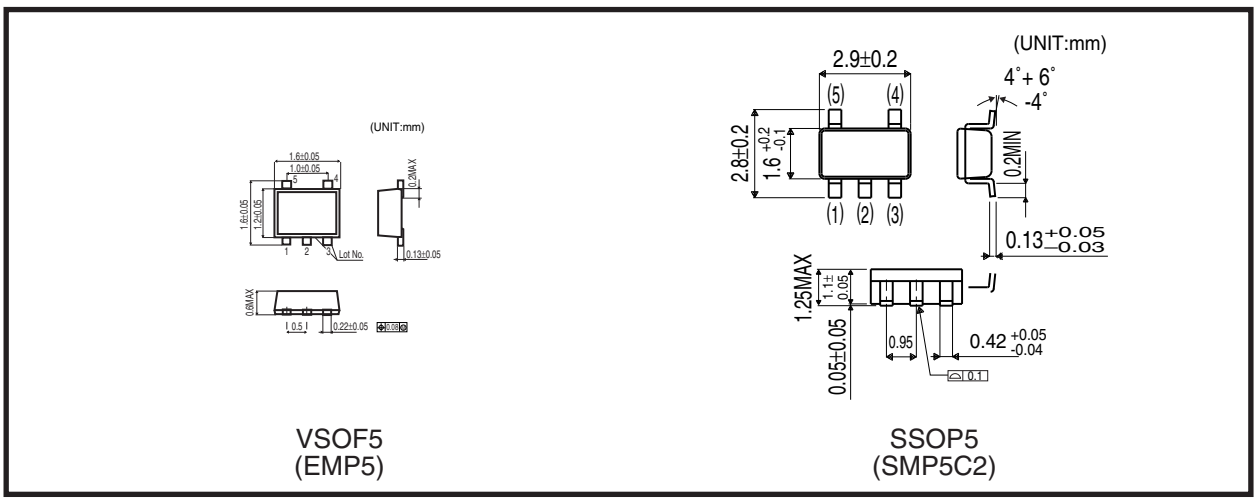
2)Flow soldering

Treatment process	Condition	
	Temperature	Time
Preheating section	150±10˚C	60~120s
Solder bath	Max. 260˚C	Max. 10s

3)Product storage conditions

Store the products in an environment of 5~30˚C in temperature and 70% RH or lower in humidity.

●Dimension



● Reference land pattern

VSOF5
(EMP5)

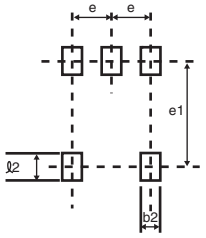


Fig.42

SSOP5
(SMP5C2)

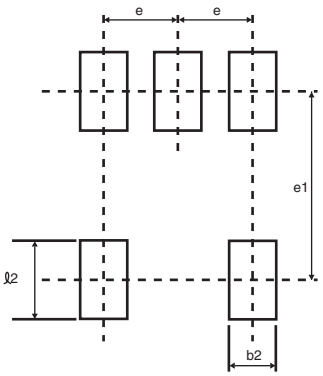


Fig.43

Unit:mm

Lead pitch e	Lead pitch e1	Land length ≧ℓ2	Land width b2
0.50	1.35	0.35	0.25

Unit:mm

Lead pitch e	Lead pitch e1	Land length ≧ℓ2	Land width b2
0.95	2.40	1.00	0.60

For actual designing, take the board density, mountability, dimension tolerance, etc. for optimization.

● Part number and marking of samples

The BD48XX and BD49XX series products allow optimum selection of detection voltage, output circuit type and package according to the application.

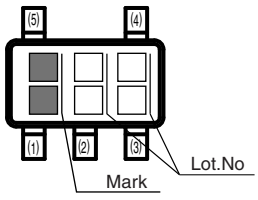
Part No.

B D 4 X X X X
① ② ③

Part No.	Specification	Contents
①	Output circuit type	8 : Open drain output 9 : CMOS output
②	Detection voltage	Ex : Vs : described in each 0.1V step for 2.3V~6.0V range (29 means 2.9V)
③	Package	G : SSOP5 (SMP5C2) FVE : VSOF5 (EMP5)

Marking	Voltage	Part No.	Marking	Voltage	Part No.	Marking	Voltage	Part No.	Marking	Voltage	Part No.
EW	6.0V	BD4860	EB	4.1V	BD4841	GW	6.0V	BD4960	GB	4.1V	BD4941
EV	5.9V	BD4859	EA	4.0V	BD4840	GV	5.9V	BD4959	GA	4.0V	BD4940
EU	5.8V	BD4858	DV	3.9V	BD4839	GU	5.8V	BD4958	FV	3.9V	BD4939
ET	5.7V	BD4857	DU	3.8V	BD4838	GT	5.7V	BD4957	FU	3.8V	BD4938
ES	5.6V	BD4856	DT	3.7V	BD4837	GS	5.6V	BD4956	FT	3.7V	BD4937
ER	5.5V	BD4855	DS	3.6V	BD4836	GR	5.5V	BD4955	FS	3.6V	BD4936
EQ	5.4V	BD4854	DR	3.5V	BD4835	GQ	5.4V	BD4954	FR	3.5V	BD4935
EP	5.3V	BD4853	DQ	3.4V	BD4834	GP	5.3V	BD4953	FQ	3.4V	BD4934
EN	5.2V	BD4852	DP	3.3V	BD4833	GN	5.2V	BD4952	FP	3.3V	BD4933
EM	5.1V	BD4851	DN	3.2V	BD4832	GM	5.1V	BD4951	FN	3.2V	BD4932
EL	5.0V	BD4850	DM	3.1V	BD4831	GL	5.0V	BD4950	FM	3.1V	BD4931
EK	4.9V	BD4849	DL	3.0V	BD4830	GK	4.9V	BD4949	FL	3.0V	BD4930
EJ	4.8V	BD4848	DK	2.9V	BD4829	GJ	4.8V	BD4948	FK	2.9V	BD4929
EH	4.7V	BD4847	DJ	2.8V	BD4828	GH	4.7V	BD4947	FJ	2.8V	BD4928
EG	4.6V	BD4846	DH	2.7V	BD4827	GG	4.6V	BD4946	FH	2.7V	BD4927
EF	4.5V	BD4845	DG	2.6V	BD4826	GF	4.5V	BD4945	FG	2.6V	BD4926
EE	4.4V	BD4844	DF	2.5V	BD4825	GE	4.4V	BD4944	FF	2.5V	BD4925
ED	4.3V	BD4843	DE	2.4V	BD4824	GD	4.3V	BD4943	FE	2.4V	BD4924
EC	4.2V	BD4842	DD	2.3V	BD4823	GC	4.2V	BD4942	FD	2.3V	BD4923

BD48XXG/BD49XXG
SSOP5 (SMP5C2)



BD48XXFVE/BD49XXFVE
VSOF5 (EMP5)